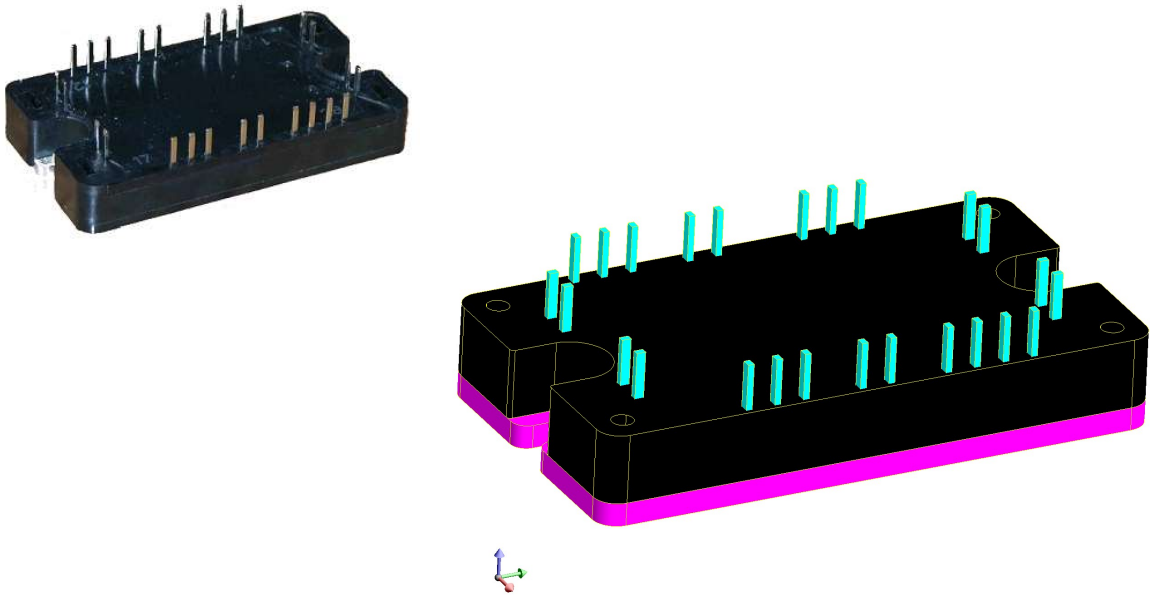
CAD package for conductor impedance
and near field simulations of electrical connections

Altair Flux™

Power module tutorial

PEEC technical example



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This technical example was edited on 12 August 2021

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Foreword

*(Please read before starting this tutorial)

Description of the document

This technical example explains all steps to model the interconnection system inside a power electronic module using the Flux PEEC software. It also contains all the data needed to describe the geometry, physics, meshing and analyze the obtained computation results.

Reference files

The Flux PEEC projects corresponding to the different cases studied in this technical example are not directly provided to the user, nevertheless he can easily create them by running the command files, written in Python language, available in the folder:
…\flux\Flux\DocExamples\ExamplesPEEC\Tutorial_Technical\PowerModule\PowerModule.zip

In particular, in the subfolder ***PowerModule_PEEC_Case1***, the following main Python files are provided:

Name	Content
buildGeo.py	Commands to automatically create the Flux PEEC project containing the description of the geometry of the studied system. It corresponds to what is described in section 2.1 and 2.2 of this tutorial.
buildPhys.py	Commands to automatically add the physics description of the studied system to an existing Flux PEEC project. It corresponds to what is described in section 2.3 of this tutorial.
State_Phys.py	Commands to automatically create the Flux PEEC project containing the description of the geometry and the physics of the studied system. It corresponds to what is described in chapter 2 of this tutorial.
State_Circuit.py	Commands to automatically create the Flux PEEC project containing the description of the geometry, the physics and the meshing, as well as the circuit of the studied system. It corresponds to what is described in chapters 2 and 3 of this tutorial.

In the subfolder ***PowerModule_PEEC_Case2***, the following main Python file is provided:

Name	Content
buildCircuit2.py	Commands to automatically add the description of the dielectrics, the capacitive regions and the computation of the capacitance matrices for the studied system to an existing Flux PEEC project. It corresponds to what is described in section 5.1 to 5.4 of this tutorial.

TABLE OF CONTENTS

1. Overview of the studied problem

Introduction

The aim of this technical paper is to better understand how to model the interconnections inside a power electronic module using the Flux PEEC software package.

This chapter contains a brief description of the device and introduces the theoretical aspects of the modeling procedure.

Contents

This chapter deals with the following topics:

1.1. Description of the device

Studied device

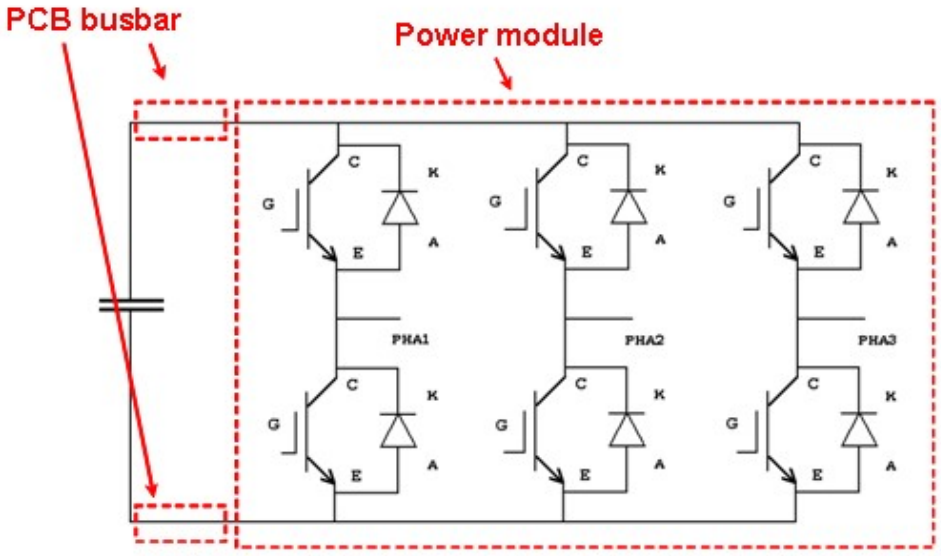
The studied device is a power electronic module dedicated to a three-phase inverter.

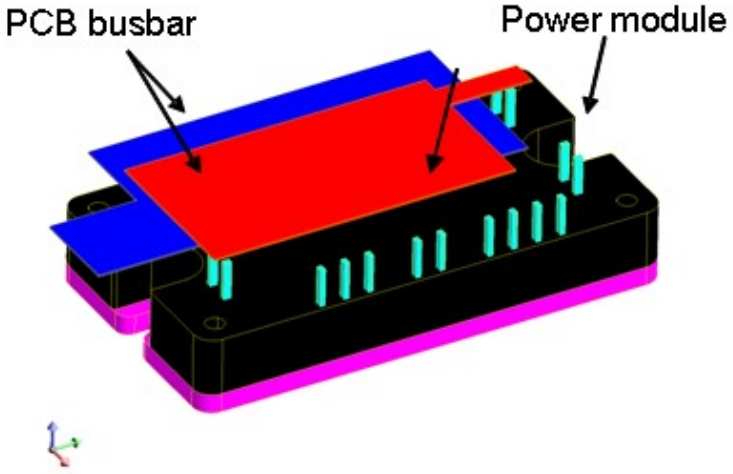
Electrical description of the device

This power electronic module (600V – 75 Amp nominal current) is a complete three-phase inverter, supplied by a DC line and providing three AC output lines, with six gate pins dedicated to the control. It is designed for AC motor control, and its maximum switching frequency is 20 kHz.

The three-phase inverter uses twelve components (six IGBT and six diodes) to realize six switching functions.

An input capacitor is used to minimize the voltage fluctuations.





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Geometry and physics

A resin is used to:

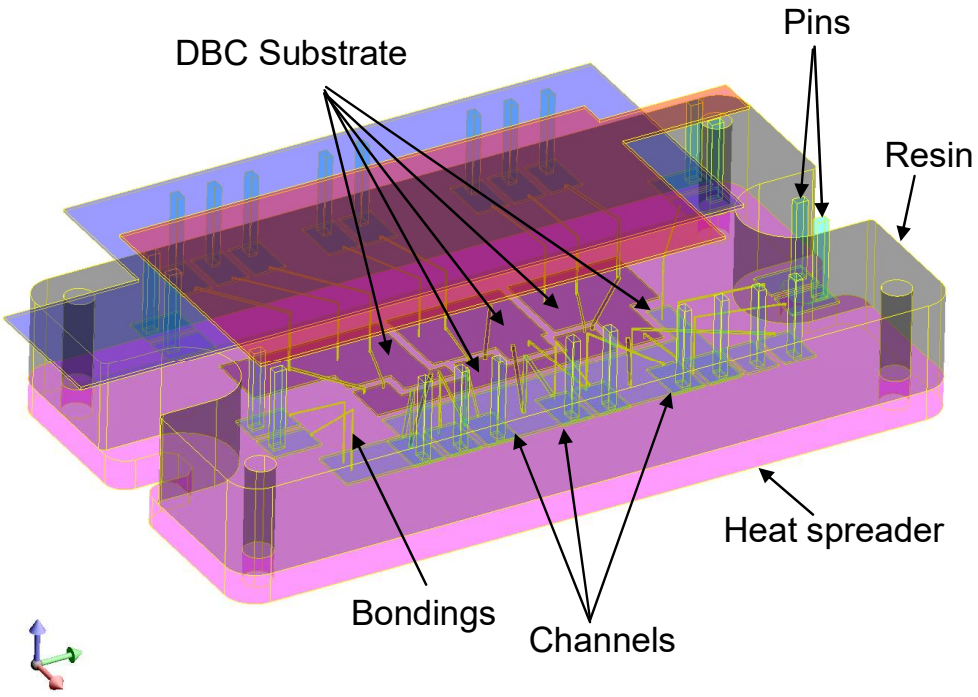
- protect the electronic part against attacks from the external environment
- improve and insure the mechanical stability
- insure the electrical isolation
- guarantee a good thermal conductivity

Each conducting part of the power electronic module is modeled in this tutorial.

Geometry of pins, channels, PCB busbar, bondings, DBC substrate (Direct Bonded Copper) and heat spreader is described in the Flux PEEC environment.

The heat spreader is not electrically connected to the other conductors, but it is considered like a ground plane and cannot be neglected, because eddy currents are induced inside by the rest of the structure. Moreover, capacitive couplings between this heat spreader and other internal conductors exist and generate common-mode currents which are one of the major causes of EMC issues.

The studied device is presented in the figure below.



Materials

The conductors of this module are made of **copper**, an electro-conductive nonmagnetic material.

Material	Resistivity (20°C)
Copper	$\rho_{Cu} = 1{,}72.10^{-8}\ \Omega.m$

1.2. Theoretical aspects

Introduction

Flux PEEC is a tool dedicated to the design of power electronic modules. Impedance models of the structures can be easily computed. As a consequence, the design can be optimized to reduce parasitic effects like unbalanced currents involved by the parasitic inductances of the geometry or voltage overshoot in semiconductors. Moreover, parasitic resistances produce additional losses. They must be dissipated by a cooling system to avoid a failure.

Such kind of modeling makes it possible a more accurate evaluation of the current and voltage constraints on the components.

In this application the value of the switching loop impedances will be evaluated.

"Conductor impedances" application

Since Flux PEEC is based on a numerical approach, conductors have to be meshed and the PEEC computation gives the partial resistances and partial self-inductances (R, L) of each element (mesh) of the conductors, plus the partial mutual couplings (M) between all the elements of the conductors.

The Flux PEEC application called "Conductor impedances with capacitive effects" also evaluate the parasitic capacitances (C) between conductors.

Then, equivalent impedances of the structure are computed by properly connecting impedance probes, which also enable to get loop inductances and resonances of the structure.

Results with Portunus

Flux PEEC can be coupled with the circuit simulation software Portunus. The impedance model is extracted from Flux PEEC as a macroblock.

Thanks to a dedicated import function in Portunus, the cabling can then be considered as a "standard" component (like diodes) and invoked to build the complete electric scheme of the device.

The evaluation of parasitic effects due to the cabling, like voltage overshoots at IGBT turn-off, can be made with the time-domain waveforms obtained with Portunus.

General process

The general process of Flux PEEC modeling is presented in the below table.

Stage	Description
1	Choice of an application and definition of a scenario
2	Conductors description
3	Electric circuit description (impedance probes)
4	Meshing
5	Solving process (according to the defined scenario)
6	Results post-processing

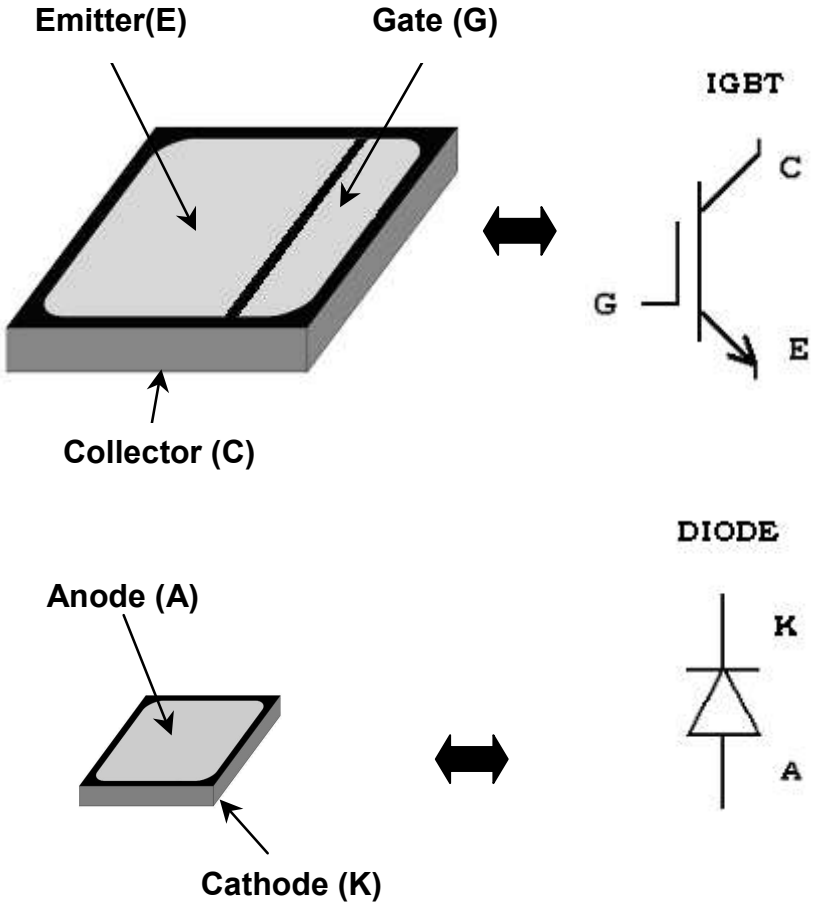
Continued on next page

The equivalent frequency

Impedances depend on the solving frequency. For this study, the frequency is set to 1 MHz. This value is deduced from the switching rise/fall times usually observed in this type of power modules. The choice is based on the fact that parasitic inductances can be neglected at the nominal working frequency (dozens of kilohertz) but not during the switching rises and falls.

Description of components

The three-phase inverter uses two types of components: IGBT and diodes. The packages show how the power electronic module is made. They are shown in the figure below.



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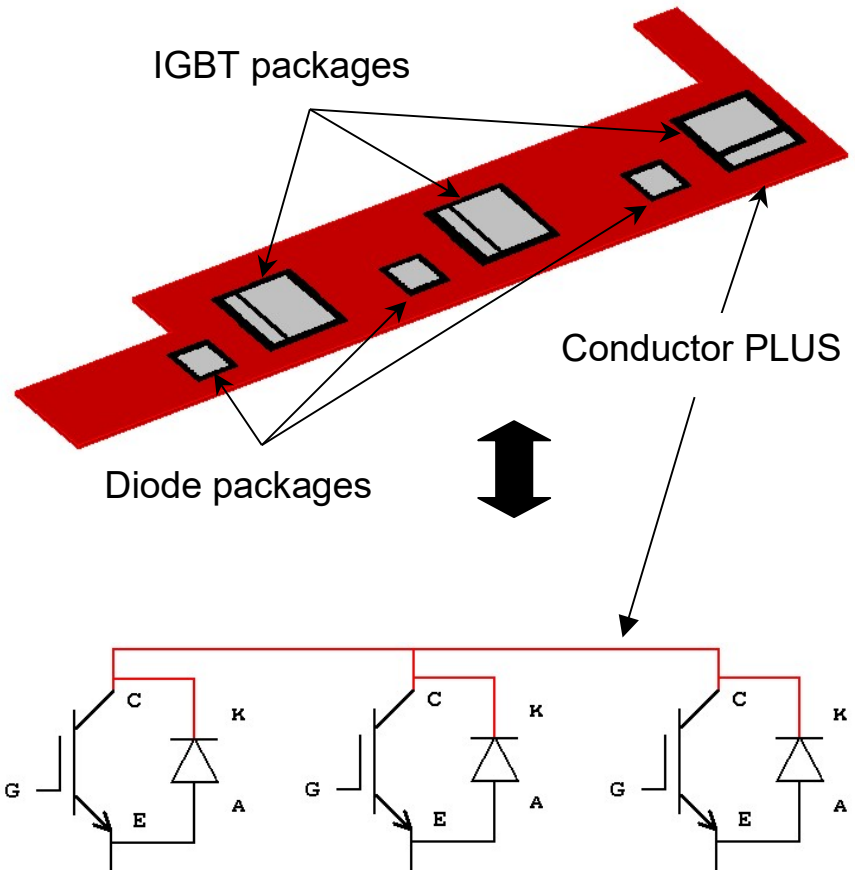
Description of the module (1)

The figure below presents one part of the module topology according to its electrical scheme.

As shown above, bottom part of IGBT and diode packages corresponds to the collector (C) and to the cathode (K), respectively. Consequently, the cathode of the three diodes and the collector of the three IGBT are welded on the conductor PLUS.

Please note that diodes and IGBT packages are not modeled in this project. Footprints are represented on the figure below only to explain the topology.



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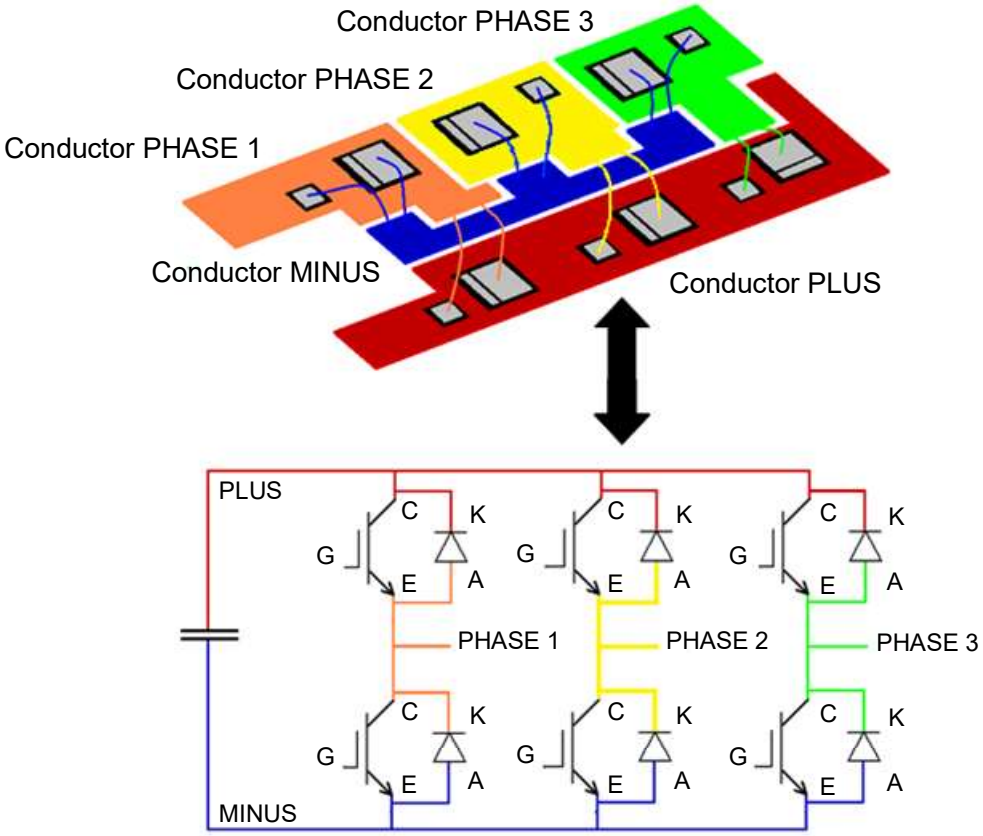
Description of the module (2)

The figure below shows the entire power module topology according to the electrical scheme.



1.3. Studied case

Studied case

Resistive, inductive and capacitive models of the studied power electronic module are generated with Flux PEEC. The modeling method is named PEEC (Partial Element Equivalent Circuit).

In the first part the loop inductances are deduced from the model. In the second part of this tutorial (chapter 5), parasitic capacitances will also be included in the model to evaluate the frequency of the electrical resonances of the structure.

Introduction

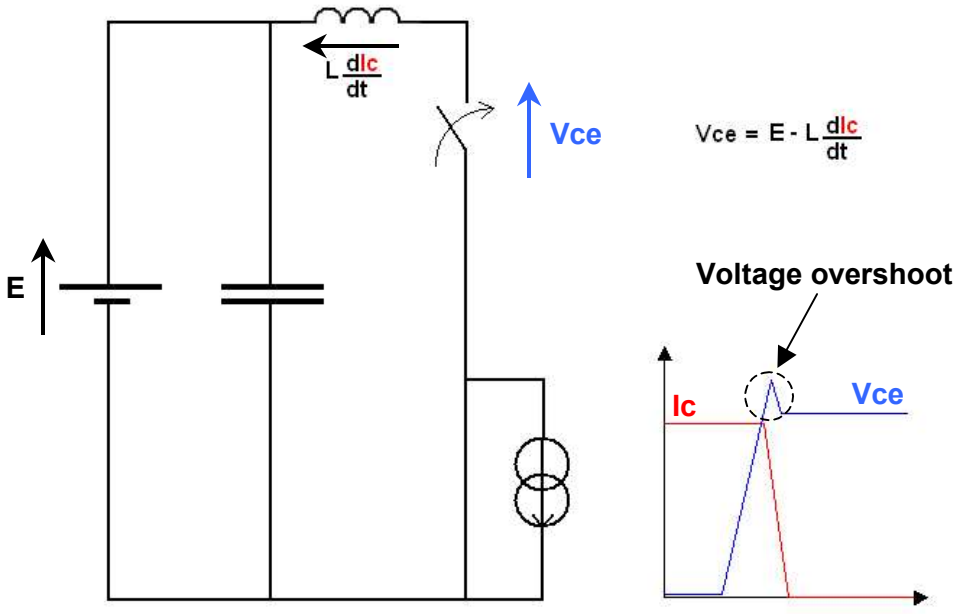
This section explains how to get switching loop inductances and what their effects are.

Capacitance effects with resonances will be introduced in the final part of this document.

Description of the switching loop inductance effect

At the instant of the IGBT turn-on, a voltage overshoot appears between collector and emitter (Vce), due to the switching loop inductance.

An important part of it comes from the parasitic inductance of the cabling.



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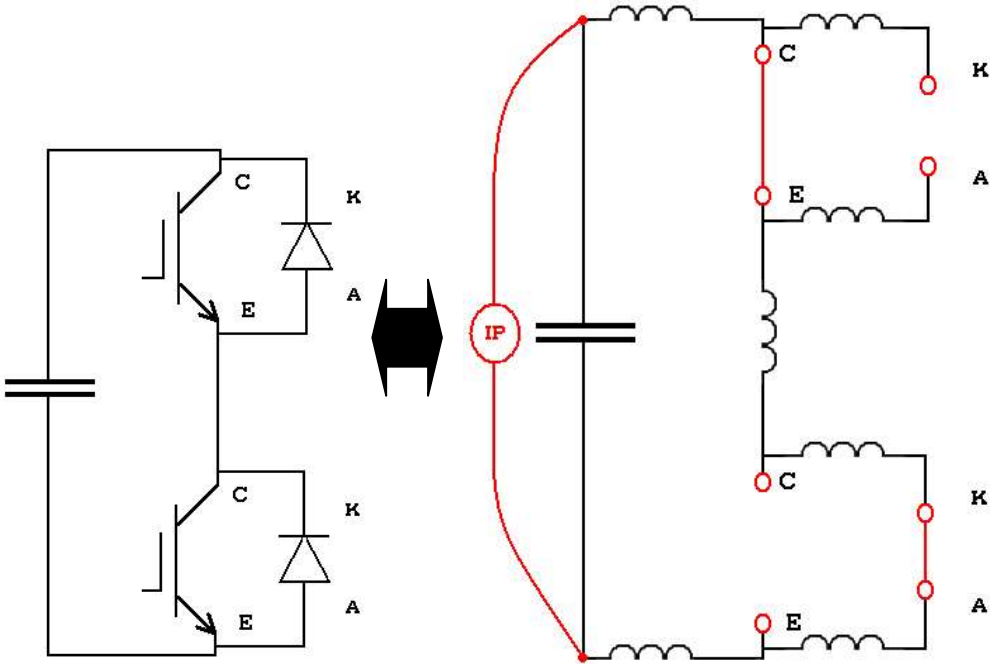
Description of the method

To get the switching loop impedance, a couple of complementary diode/IGBT is short-circuited and one impedance probe is used to compute the impedance. To get the six switching loop impedances, this operation is done for each of the six couples.



2. Application, geometry, physics and meshing of conductors

Introduction

This chapter presents the application, the geometry import with the associated physics and the meshing of the power electronic module.

Python file

The reader willing to skip this part of the tutorial and to directly move to the next chapter 3 can easily generate the Flux PEEC project containing the geometry, the physics and the meshing of the studied system by running the Python file ***State_Phys.py*** provided in the folder ***…\flux\Flux\DocExamples\ExamplesPEEC\Tutorial_Technical\PowerModule\PowerModule.zip\PowerModule_PEEC_Case1***

In the same manner, the reader willing to move to the definition of the physics (paragraph 2.3) has just to run the Python file ***buildGeo.py*** provided in the same folder indicated above.

Overview

The application, geometry, physics and meshing descriptions will be realized in four steps described in the table below.

Stage	Description
1	Choice and definition of the suitable application
2	Geometry import
3	Definition of the physics
4	Meshing

Contents

This chapter deals with the following topics:

2.1. Choice and definition of the application

Introduction This section presents the physical definition of the application.

Contents This section deals with the following topics:

2.1.1. Start and define physics for the application

Goal

First, the Flux PEEC application is defined to compute the resistive and inductive models.

Definition of the application

The suitable application is **Conductor impedances**.
Properties to be set are presented in the table below.

Type of application	Default material for new conductors
Conductor impedances	copper

2.1.2. Define the scenario of the solving process

Goal

The value of frequency (1 MHz) for the solving process is set via the solving scenario (only one scenario by project).

Definition of the scenario

Properties of the scenario are reported in the table below.

Name	Parameter controlled	Control type	Value
Scenario_1	FREQUENCY	Mono-value	1e6

2.2. Geometry import

Introduction

This section presents how to describe the geometry of the module by means of an imported CAD file.

Contents

This section deals with the following topics:

2.2.1. CAD import

Goal

Import the geometry into Flux PEEC.

Action (1)

The geometry description of the power module is provided under the form of a MCAD (Mechanical Computer-Aided Design) file. The corresponding SAT file (**PowerModule_Geometry.SAT**) is supplied to the user in the folder ***…\flux\Flux\DocExamples\ExamplesPEEC\Tutorial_Technical\PowerModule\PowerModule.zip\PowerModule_PEEC_Case1***

Properties of the CAD import are reported in the table below.

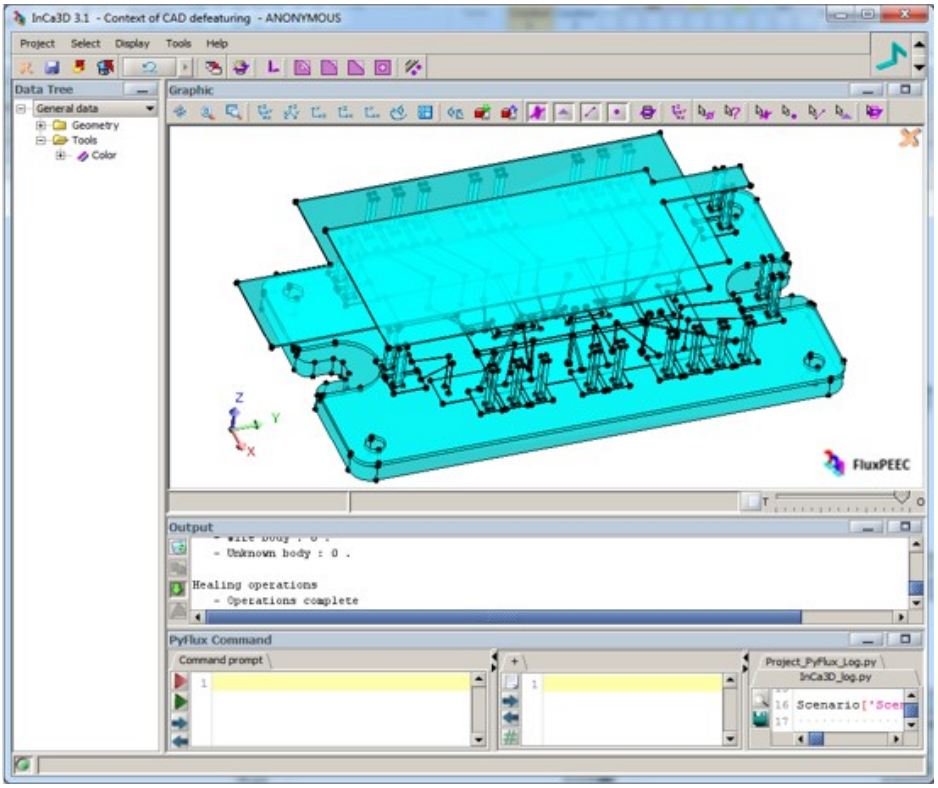
File name	File format	Coordinate system	Automatic healing
PowerModule_Geometry	SAT	XYZ1	Yes

☞ **Project → CAD import → Import of a SAT file**

Result (1)

The geometry is imported into the **context of CAD defeaturing**, which is used to clean the geometry if necessary: holes, chamfers and blends can be easily suppressed with defeaturing tools available in Flux PEEC. These suppressions are often requested to simplify the meshing.

The imported geometry into this environment is shown in the below figure; it is composed of one hundred and eighty objects.



2.2.2. Defeaturing

Goal

Simplify the geometry using the defeaturing tools in order to easily mesh the structure to be simulated.

Diameter computation

With the aim of making its meshing easier, the heat spreader (**OBJECT_IMPORT_167**) and the resin layer (**OBJECT_IMPORT_176**) need to be simplified: in fact, holes, blends and chamfers exist in these pieces.

To prepare defeaturing operations, the diameter of the heat spreader holes is computed.

First top sub entity to get distance	Second top sub entity	Coordinate system for top distance
1561	1562	XYZ1

☞ **Tools → Compute distance between two top sub entities** 

Result (1)

Distance is equal to 2.828 mm.

Hole suppression

All the four holes of the heat spreader and the four of the resin layer are suppressed.

Properties for this suppression are presented in the table below: the default value of 0.0050 m for the maximum diameter can be left, because it is bigger than the hole size.

Diameter max for holes remove (meter)	Objects to defeature
0.0050	OBJECT_IMPORT_167 OBJECT_IMPORT_176

☞ **Tools → Make a hole defeaturing** 

Width computation

To prepare the treatment of heat spreader chamfers, their width is computed.

First top sub entity to get distance	Second top sub entity	Coordinate system for top distance
1563	1562	XYZ1

☞ **Tools → Compute distance between two top sub entities** 

Result (2)

Distance is equal to 1.414 mm.

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Chamfer suppression

All the four chamfers of the heat spreader are suppressed.

Properties for this suppression are presented in the table below: the default value of 0.0050 m for the maximum width can be left, because it is bigger than the chamfer size.

Width max for chamfers remove (meter)	Objects to defeature
0.0050	OBJECT_IMPORT_167

☞ Tools → Make a chamfer defeaturing 

Radius estimation

To prepare the treatment of blends on heat spreader and on resin layer, their radius is estimated by computing the chord length between the two points that define the blend.

OBJECT_IMPORT_167 and **OBJECT_IMPORT_176** present three dimensions of blend: chord is computed for all of them.

☞ Tools → Compute distance between two top sub entities 

Blend number	First top sub entity to get distance	Second top sub entity	Coordinate system for top distance
1	1583	1584	XYZ1
2	1582	1581	XYZ1
3	1611	1612	XYZ1

Result (3)

Chord distances are equal to 2.828 mm, 4.243 mm and 0.707 mm, respectively.

Since in this case all blends present an angle of 90°, their radius can be estimated by simply dividing the chord distance by $\sqrt{2}$. Obtained values are then 2 mm, 3 mm and 0.5 mm, respectively.

Blend suppression

All the eight blends of the heat spreader and all the eight ones of the resin layer are suppressed.

Properties for this suppression are presented in the table below: default values are adequate for the maximum angle, but not suitable for radius, because it is smaller than the blend size. It is consequently changed to 0.0050 m.

Radius max for blends remove (meter)	Angle max for blends remove (degree)	Objects to defeature
0.0050	175	OBJECT_IMPORT_167 OBJECT_IMPORT_176

☞ Tools → Make a blend defeaturing 

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Standard Flux PEEC context

Import and defeaturing operations are now concluded and the user can quit the dedicated context and come back to the standard Flux PEEC window to carry on with the physical description of the simulation.

☞	Project → Return to standard geometry context	

Result (4)

The imported objects are converted in 1176 points, 1946 lines, 1040 faces and 180 volumes that define the entire geometry to simulate.

Appearance

For a better visualization of all points and lines, their color is modified from turquoise to white.

☞	Geometry → Assimilation geometry → Point → Edit	

☞	Geometry → Assimilation geometry → Line → Edit	

2.3. Physics and meshing

Introduction This section describes the physics associated to the imported geometry.

Python file The reader willing to skip this part of the tutorial and to directly move to the next chapter 3 has just to run the Python file ***buildPhys.py*** provided in the folder
…\flux\Flux\DocExamples\ExamplesPEEC\Tutorial_Technical\PowerModule\PowerModule.zip\PowerModule_PEEC_Case1

Contents This section deals with the following topics:

2.3.1. Physics of bondings

Goal

Bondings are conductors connecting channels and DBC substrate to IGBT and diodes. Because of their shape (similar to cables), a privileged path for the electric current can be identified. Consequently, from a physical point of view they are considered like unidirectional conductors.

Data

The properties of the thirty-two unidirectional conductors associated to bondings are presented in the table below.

Unidirectional conductors defined from classic geometry description			
Name	**Description**		
	List of volumes	**List of input faces**	**List of output faces**
BOND_1	79, 75, 74	410	434
BOND_2	73, 68, 69	377	401
BOND_3	13, 9, 8	46	70
BOND_4	62, 66, 67	344	368
BOND_5	7, 3, 2	13	37
BOND_6	112, 108, 107	592	616
BOND_7	61, 57, 56	311	335
BOND_8	49, 45, 44	244	268
BOND_9	103, 99, 98	542	566
BOND_10	135, 131, 130	957	981
BOND_11	43, 39, 38	211	235
BOND_12	97, 93, 92	509	533
BOND_13	37, 33, 32	178	202
BOND_14	91, 87, 86	476	500
BOND_15	31, 27, 26	145	169
BOND_16	85, 81, 80	443	467
BOND_17	25, 21, 20	112	136
BOND_18	19, 15, 14	79	103
BOND_19	129, 125, 143	990	909
BOND_20	141, 137, 136	914	942
BOND_21	172, 171, 170	739	748
BOND_22	176, 175, 174	711	724
BOND_23	124, 123, 122	1016	1025
BOND_24	121, 120, 180	1030	669
BOND_25	165, 164, 163	781	790
BOND_26	169, 168, 167	755	768
BOND_27	152, 151, 150	859	868
BOND_28	155, 154, 153	843	852
BOND_29	149, 148, 147	875	884
BOND_30	162, 161, 159	795	824
BOND_31	158, 157, 156	827	836
BOND_32	146, 145, 144	891	900

☞ **Physics → Unidirectional conductor → New** 

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Meshing

By default, properties for the meshing of these 32 unidirectional conductors are set to ***"according to the solving configuration"***. Considering the studied device and in order to avoid useless elements, meshing strategy is modified: a uniform distribution of elements for the cross-section is defined for all conductors that model the bondings, by editing the tab "**Meshing**" of the corresponding entities.

Data

Modified properties of the conductors are reported in the table below.

Unidirectional conductors defined from classic geometry description				
Name	**Meshing**			
	Section			**Length**
	Type	**Minimum number of elements**		
		Side 1	**Side 2**	
BOND_1 to BOND_32	Uniform regular	1	1	1

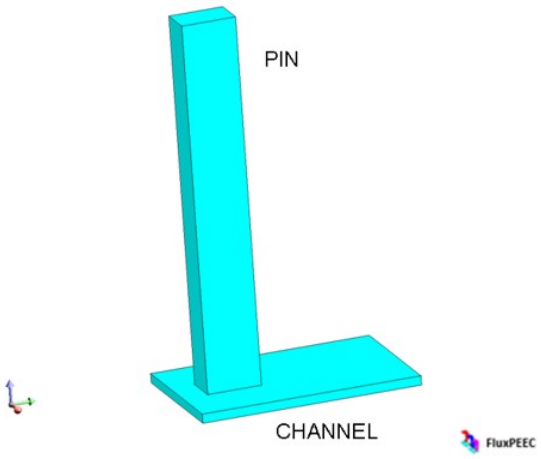
☞ **Physics → Unidirectional conductor → Edit array** 

2.3.2. Physics of pins and channels

Goal

The studied power module is composed of twenty-five pairs of pins and channels; nevertheless five of them can be ignored in this simulation since they are devoted to control and sensor signals. Consequently, volumes of only twenty pairs are associated to conductors in order to define the flow of the current inside them.

In particular, pins are described as unidirectional conductors, while channels need to be considered as bidirectional conductors due to their shape analogous to a plane.



Pins

The properties of the twenty unidirectional conductors associated to the pins are presented in the table below.

Unidirectional conductors defined from classic geometry description						
Name	**Description**			**Meshing**		
				Uniform regular		
				Section		**Length**
	List of volumes	**List of input faces**	**List of output faces**	**Side 1**	**Side 2**	
PIN_1	77	419	427	2	1	1
PIN_2	70	392	390	2	1	1
PIN_3	10	61	59	2	1	1
PIN_4	65	359	357	2	1	1
PIN_5	4	28	26	2	1	1
PIN_6	109	607	605	2	1	1
PIN_9	58	326	324	2	1	1
PIN_10	46	259	257	1	2	1
PIN_11	100	557	555	1	2	1
PIN_12	132	970	972	1	2	1
PIN_14	41	220	228	2	1	1
PIN_15	94	522	524	2	1	1
PIN_16	34	191	193	2	1	1
PIN_17	88	491	489	2	1	1
PIN_18	28	160	158	2	1	1

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Unidirectional conductors defined from classic geometry description						
Name	**Description**			**Meshing**		
	List of volumes	**List of input faces**	**List of output faces**	**Uniform regular**		
				Section		**Length**
				Side 1	**Side 2**	
PIN_19	82	458	456	2	1	1
PIN_20	22	125	127	2	1	1
PIN_21	16	92	94	2	1	1
PIN_24	126	1003	1005	1	2	1
PIN_25	138	927	929	1	2	1

☞ **Physics → Unidirectional conductor → New** 

Channels

The properties of the twenty bidirectional conductors associated to the channels are presented in the table below.

Bidirectional conductor defined by a **list of volumes**						
Name	**Description**		**Meshing**			
	List of volumes	**Face of definition of the current flow plane**	**Surface**			**Thickness**
			Type	**Side 1**	**Side 2**	
CH_1	78, 76	411	Uniform - Piecewise	3	3	None, i.e. one element
CH_2	72, 71	383	Uniform - Piecewise	3	3	None, i.e. one element
CH_3	12, 11	47	Uniform - Piecewise	3	3	None, i.e. one element
CH_4	63, 64	350	Uniform - Piecewise	3	3	None, i.e. one element
CH_5	6, 5	14	Uniform - Piecewise	3	3	None, i.e. one element
CH_6	111, 110	593	Uniform - Piecewise	3	3	None, i.e. one element
CH_9	60, 59	312	Uniform - Piecewise	3	3	None, i.e. one element
CH_10	48, 47	245	Uniform - Piecewise	3	3	None, i.e. one element
CH_11	102, 101	543	Uniform - Piecewise	3	3	None, i.e. one element
CH_12	134, 133	958	Uniform - Piecewise	3	3	None, i.e. one element
CH_14	42, 40	212	Uniform - Piecewise	3	3	None, i.e. one element
CH_15	96, 95	515	Uniform - Piecewise	3	3	None, i.e. one element
CH_16	36, 35	179	Uniform - Piecewise	3	3	None, i.e. one element

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Bidirectional conductor defined by a **list of volumes**						
Name	**Description**		**Meshing**			
	List of volumes	**Face of definition of the current flow plane**	**Surface**			**Thickness**
			Type	**Side 1**	**Side 2**	
CH_17	90, 89	477	Uniform - Piecewise	3	3	None, i.e. one element
CH_18	30, 29	146	Uniform - Piecewise	3	3	None, i.e. one element
CH_19	84, 83	449	Uniform - Piecewise	3	3	None, i.e. one element
CH_20	24, 23	113	Uniform - Piecewise	3	3	None, i.e. one element
CH_21	18, 17	80	Uniform - Piecewise	3	3	None, i.e. one element
CH_24	128, 127	996	Uniform - Piecewise	3	3	None, i.e. one element
CH_25	140, 139	915	Uniform - Piecewise	3	3	None, i.e. one element

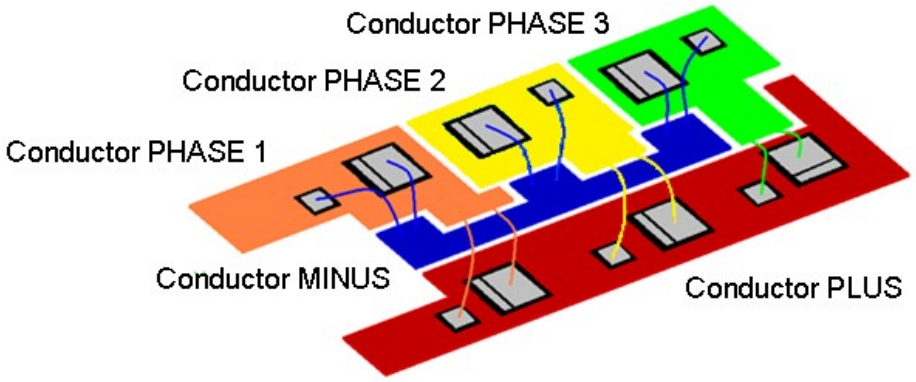
☞ **Physics → Bidirectional conductor → New** 

2.3.3. Physics of DBC substrate, heat spreader and PCB busbars

Goal

The shape of the volumes associated to DBC substrate, heat spreader and PCB busbars requires bidirectional conductors to properly model the current flow.

Eight conductors are consequently defined: five of them are related to the DBC substrate, as indicated in the below figure.



Data

The properties of bidirectional conductors are reported in the table below.

Bidirectional conductor defined by a **list of volumes**							
Name	**Description**		**Meshing**				**Appearance**
	List of volumes	**Face of definition of the current flow plane**	**Surface**			**Thickness**	**Color**
			Type	**Side 1**	**Side 2**		
PHASE1	173	725	Uniform - Piecewise	5	12	None, i.e. one element	Orange
PHASE2	179	670	Uniform - Piecewise	5	8	None, i.e. one element	Yellow
PHASE3	166	769	Uniform - Piecewise	7	9	None, i.e. one element	Green
MINUS	160	805	Uniform - Piecewise	4	12	None, i.e. one element	Blue
PLUS	142	943	Uniform - Piecewise	6	24	None, i.e. one element	Red
HEAT	177	695	Uniform - Piecewise	25	20	Uniform - 2 elements	Magenta
PCB_P	119	655	Uniform - Piecewise	14	17	None, i.e. one element	Red
PCB_M	1	1	Uniform - Piecewise	14	20	None, i.e. one element	Blue

☞ **Physics → Bidirectional conductor → New** 

2.3.4. Generate the meshing

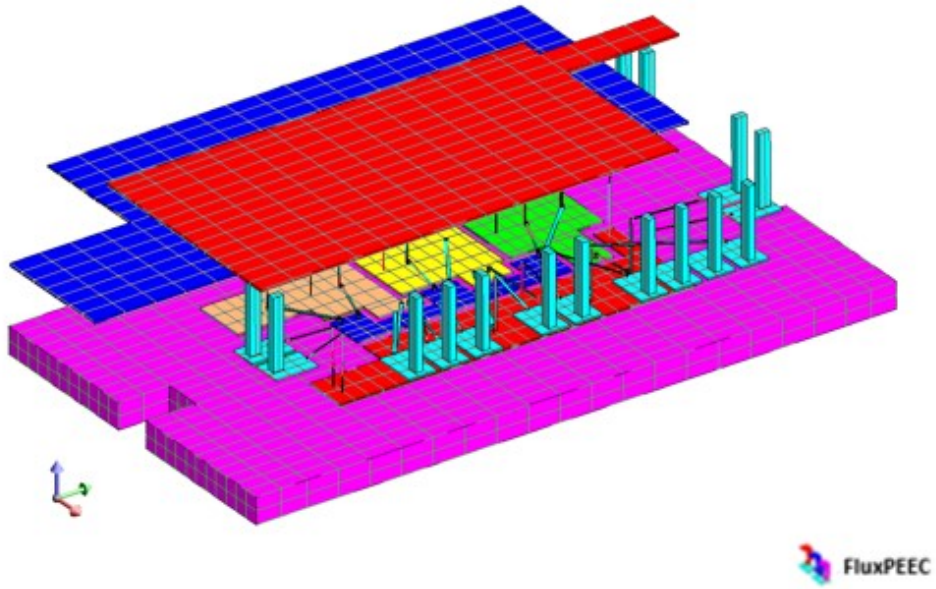
Action

The meshing of the power electronic module is generated using the **Mesh** command.

☞	Solving → Mesh	

Result

Obtained meshing is shown in the figure below.



3. Electric circuit

Introduction

This chapter shows how to build the electric circuit associated to the power electronic module.

For the cases studied in the first part of this tutorial, the electric circuit is made up of:

- conductors, defined in the previous section
- impedance probes for the extraction of loop inductances of the structure
- electrical connections (carried out via the terminals) between conductors and probes.

Python file

The reader willing to skip this part of the tutorial and to directly move to the next section can easily generate the Flux PEEC project containing the circuit description of the studied system by running the Python file ***buildCircuit.py*** provided in the folder
…\flux\Flux\DocExamples\ExamplesPEEC\Tutorial_Technical\PowerModule\PowerModule.zip\PowerModule_PEEC_Case1

Overview

The electric circuit description will be realized in three steps listed in the table below.

Stage	Description
1	Creation of terminals
2	Manual creation of connections
3	Creation and automatic connection of impedance probes

Contents

This chapter deals with the following topics:

3.1. Creation of terminals

Goal

The aim of this section is the creation of the terminals necessary for the establishment of the electric circuit of the power module.

Automatic creation of terminals

Terminals associated to unidirectional conductors (modeling both bondings and pins) are automatically created by Flux PEEC in order to help the user.

They are labeled with the conductor's name followed by a suffix which indicates their place along the conductor. For example, TERM_BOND_1_1 is the first terminal of the conductor BOND_1.

In this tutorial, up to now 168 terminals have been created by Flux PEEC: they are associated to bondings and pins because they have been previously described as unidirectional conductors.

Bidirectional conductors

Terminals for bidirectional conductors have to be manually created by the user, as described in the following blocks:

Contents

This section deals with the following topics:

3.1.1. Terminals of PHASE1, PHASE2 and PHASE3 conductors

Goal

Terminals of bidirectional conductors can be created from points or faces. For PHASE1, PHASE2 and PHASE3 conductors of this study, it is suitable to choose point-type terminals, because they are devoted to the connection with IGBT, diodes or bondings.

Twelve new points have to be added to the geometry of DBC substrate in order to be then associated to terminals.

Data (1)

The properties of the points necessary to define the terminals of PHASE1, PHASE2 and PHASE3 conductors are reported in the table below.

Point defined by its **parametric coordinates**					
Number	**Geometric definition**				**Appearance**
	Coord. system	**Coordinates**			**Color**
		First	**Second**	**Third**	
1181	XYZ1	-7.84	-10.955	-6.3	Orange
1182		-7.3	-2.975	-6.3	
1183		-0.99	-0.275	-6.3	
1184		-0.99	0.555	-6.3	
1185		-7.5	4.905	-6.3	Yellow
1186		-8.82	10.305	-6.3	
1187		-1.96	8.725	-6.3	
1188		-1.96	10.575	-6.3	
1189		-7.28	18.275	-6.3	Green
1190		-8.06	22.985	-6.3	
1191		1.69	18.465	-6.3	
1192		1.69	20.125	-6.3	

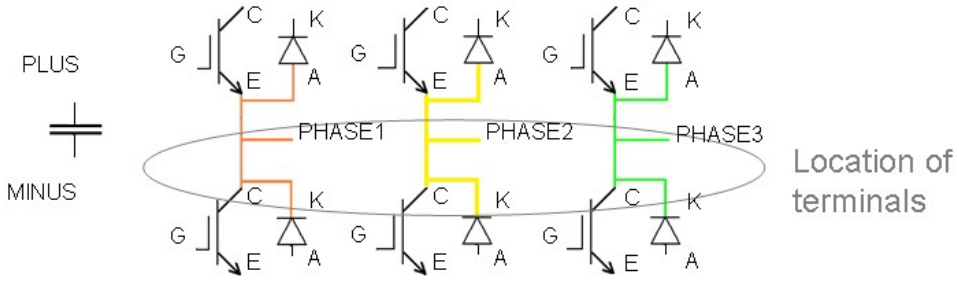
☞ **Geometry → Assimilation geometry → Point → New** 

Continued on next page

Data (2)

The properties of terminals of PHASE1, PHASE2 and PHASE3 conductors are reported in the table below.

The electrical location of these terminals is indicated in the below figure: they enable the connection with collector of the three low-side IGBT, with cathode of the three low-side diodes and with six bondings which go to external pins of the three-phase inverter.



Terminal of **bidirectional conductor**					
Name	**Definition**				**Appearance**
	Type of terminal	**Point of the terminal**	**Conductor where the terminal is located**	**Pin of macro component**	**Color**
K1L	Point	1181	PHASE1	No	Orange
C1L		1182			
PIN_1		1183			
PIN_3		1184			
C2L	Point	1185	PHASE2	No	Yellow
K2L		1186			
PIN_4		1187			
PIN_6		1188			
C3L	Point	1189	PHASE3	No	Green
K3L		1190			
PIN_9		1191			
PIN_11		1192			

☞ **Components and Electric Circuit → Terminal → New** 

Result

At the creation of these terminals, Flux PEEC has also created six equipotential connections between bondings and conductors PHASE1, PHASE2 and PHASE3: in fact, an automatic algorithm has detected all the intersections between the faces (that have terminals) of unidirectional and bidirectional conductors and added the corresponding connections.
For example, CO_AUTO_1 joins, from an electrical point-of-view, the unidirectional conductor describing the bonding BOND_21 to the bidirectional conductor PHASE1: this connection is established by means of the terminals TERM_BOND_21_4 and PIN_1.

3.1.2. Terminals of PLUS and MINUS conductors

Goal

Terminals of PLUS and MINUS conductors are created; it is suitable to choose point-type terminals, because they are devoted to the connection with IGBT, diodes or bondings.

Fifteen new points have to be added to the geometry of DBC substrate in order to be then associated to terminals.

Data (1)

The properties of the points necessary to define the terminals of PLUS and MINUS conductors are reported in the table below.

Point defined by its **parametric coordinates**					
Number	**Geometric definition**				**Appearance**
	Coord. system	**Coordinates**			**Color**
		First	**Second**	**Third**	
1193	XYZ1	9.01	-7.975	-6.3	Red
1194		7.98	-1.815	-6.3	
1195		8.43	3.935	-6.3	
1196		7.66	10.765	-6.3	
1197		8.87	14.665	-6.3	
1198		6.79	20.635	-6.3	
1199		-0.37	23.135	-6.3	
1200		8.01	-14.38	-6.3	
1201		9.47	-14.385	-6.3	
1202		-1.56	-6.795	-6.3	Blue
1203		-1.56	-4.835	-6.3	
1204		-1.74	4.065	-6.3	
1205		-1.76	5.725	-6.3	
1206		-1.68	16.735	-6.3	
1207		-1.68	15.905	-6.3	

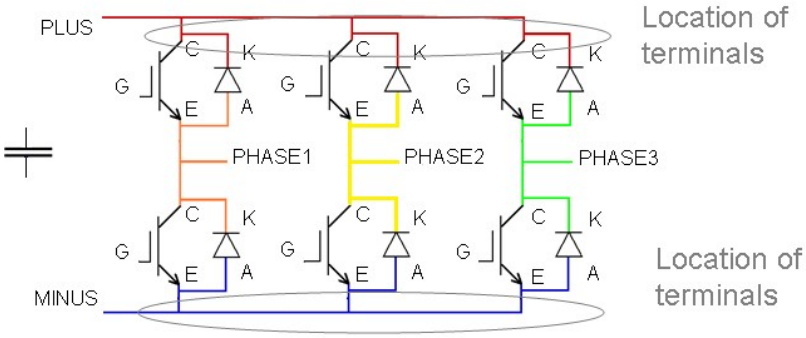
☞ **Geometry → Assimilation geometry → Point → New** 

Continued on next page

Data (2)

The properties of terminals of PLUS and MINUS conductors are reported in the table below.

The electrical location of these terminals is indicated in the figure: they enable the connection with collector of the three high-side IGBT, with cathode of the three high-side diodes, with eight bondings which go to external pins of the power module and one internal bonding.



Terminal of **bidirectional conductor**					
Name	**Definition**				**Appearance**
	Type of terminal	**Point of the terminal**	**Conductor where the terminal is located**	**Pin of macro component**	**Color**
K1H	Point	1193	PLUS	No	Red
C1H		1194			
K2H		1195			
C2H		1196			
K3H		1197			
C3H		1198			
PIN_12		1199			
PIN_24		1200			
PIN_25		1201			
PIN_21	Point	1202	MINUS	No	Blue
PIN_19		1203			
PIN_17		1204			
INT_A2L		1205			
PIN_14		1206			
PIN_15		1207			

☞ **Components and Electric Circuit → Terminal → New** 

Result

At the creation of these terminals, the algorithm for the creation of connections is automatically run and nine new equipotential connections between bondings and conductors PLUS and MINUS have been created by Flux PEEC.

3.1.3. Terminals of PCB busbars

Goal

Terminals of PCB busbars are created; most of them are point-type terminals, because they are devoted to the connection with one pin of the power module or to the negative of the input capacitor. Last terminal is face-type because it is dedicated to the connection with the positive of the capacitor bank.

Six new points have to be added to the geometry of the PCB busbars in order to be then associated to terminals.

Data (1)

The properties of the points necessary to define the terminals of PCB_P and PCB_M conductors are reported in the table below.

Point defined by its **parametric coordinates**					
Number	**Geometric definition**				**Appearance**
	Coord. system	**Coordinates**			**Color**
		First	**Second**	**Third**	
1208	XYZ1	7.62	-23.305	9.85	Red
1209		11.43	-23.305	9.85	
1210		-7.62	32.485	9.85	
1211		-19	-16.365	8.85	Blue
1212		-19	21.735	8.85	
1213		-5.2	25.545	8.85	

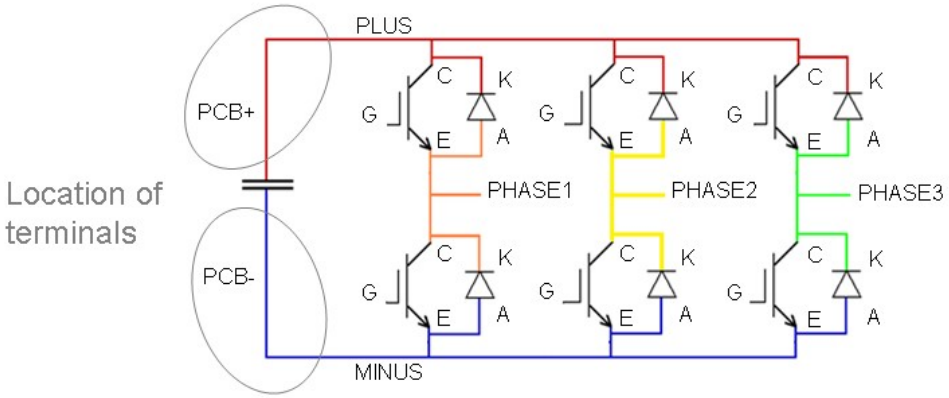
☞ **Geometry → Assimilation geometry → Point → New** 

Continued on next page

Data (2)

The properties of terminals of PCB_P and PCB_M conductors are reported in the table below.

The electrical location of these terminals is indicated in the figure: they enable the connection with capacitor bank and with three-phase inverter pins.



Terminal of bidirectional conductor					
Name	Definition				Appearance
	Type of terminal	Point or faces of the terminal	Conductor where the terminal is located	Pin of macro component	Color
PCB_P_P24	Point	1208	PCB_P	No	Red
PCB_P_P25		1209			
PCB_P_P12		1210			
PCB_P_IN	Face	659			
PCB_M_P21	Point	1211	PCB_M	No	Blue
PCB_M_P14		1212			
PCB_M_IN		1213			

☞ Components and Electric Circuit → Terminal → New 

Result

At the creation of these terminals, no new connection is created by Flux PEEC since any intersection exists between these new terminals and the existing ones. Consequently, connections for PCB_P and PCB_M conductors have to be manually built by the user.

3.1.4. Terminals of channels

Goal

Channels have to be connected to bondings on one side, and pins on the other side. Since the section of bondings is small, the point-type terminals are adequate. The face-type terminals are better suitable for the connection of channels to pins because they are larger than bondings.

Twenty new points have to be added to the geometry of the channels in order to be then associated to terminals, whereas necessary faces already exist in the Flux PEEC project.

Data (1)

The properties of the points necessary to define the terminals of channels are reported in the table below.

Point defined by its **parametric coordinates**					
Number	**Geometric definition**				**Appearance**
	Coord. system	**Coordinates**			**Color**
		First	**Second**	**Third**	
1214	XYZ1	15.48	-12.555	-0.15	White
1215		15.48	-8.745	-0.15	
1216		15.48	-4.935	-0.15	
1217		15.48	2.685	-0.15	
1218		15.48	6.495	-0.15	
1219		15.48	14.115	-0.15	
1220		15.48	25.545	-0.15	
1221		11.43	28.965	-0.15	
1222		7.62	28.965	-0.15	
1223		-7.62	28.965	-0.15	
1224		-15.48	21.735	-0.15	
1225		-15.48	17.925	-0.15	
1226		-15.48	14.115	-0.15	
1227		-15.48	2.685	-0.15	
1228		-15.48	-1.125	-0.15	
1229		-15.48	-8.745	-0.15	
1230		-15.48	-12.555	-0.15	
1231		-15.48	-16.365	-0.15	
1232		7.66	-19.78	-0.15	
1233		11.43	-19.785	-0.15	

☞ **Geometry → Assimilation geometry → Point → New** 

Continued on next page

Data (2)

The properties of terminals for the connection of channels to bondings are reported in the table below.

Terminal of bidirectional conductor					
Name	Definition				Appearance
	Type of terminal	Point of the terminal	Conductor where the terminal is located	Pin of macro component	Color
CH_BOND_1	Point	1214	CH_1	No	Turquoise
CH_BOND_2		1215	CH_2		
CH_BOND_3		1216	CH_3		
CH_BOND_4		1217	CH_4		
CH_BOND_5		1218	CH_5		
CH_BOND_6		1219	CH_6		
CH_BOND_9		1220	CH_9		
CH_BOND_10		1221	CH_10		
CH_BOND_11		1222	CH_11		
CH_BOND_12		1223	CH_12		
CH_BOND_14		1224	CH_14		
CH_BOND_15		1225	CH_15		
CH_BOND_16		1226	CH_16		
CH_BOND_17		1227	CH_17		
CH_BOND_18		1228	CH_18		
CH_BOND_19		1229	CH_19		
CH_BOND_20		1230	CH_20		
CH_BOND_21		1231	CH_21		
CH_BOND_24		1232	CH_24		
CH_BOND_25		1233	CH_25		

☞ **Components and Electric Circuit → Terminal → New** 

Result (1)

At the creation of these terminals, the algorithm for the creation of connections is automatically run and twenty new equipotential connections between bondings and channels have been created by Flux PEEC.

Continued on next page

Data (3)

The properties of terminals for the connection of channels to pins are reported in the table below.

Terminal of **bidirectional conductor**					
Name	**Definition**				**Appearance**
	Type of terminal	**Faces of the terminal**	**Conductor where the terminal is located**	**Pin of macro component**	**Color**
CH_PIN_1	Face	427	CH_1	No	Turquoise
CH_PIN_2		390	CH_2		
CH_PIN_3		59	CH_3		
CH_PIN_4		357	CH_4		
CH_PIN_5		26	CH_5		
CH_PIN_6		605	CH_6		
CH_PIN_9		324	CH_9		
CH_PIN_10		257	CH_10		
CH_PIN_11		555	CH_11		
CH_PIN_12		972	CH_12		
CH_PIN_14		228	CH_14		
CH_PIN_15		524	CH_15		
CH_PIN_16		193	CH_16		
CH_PIN_17		489	CH_17		
CH_PIN_18		158	CH_18		
CH_PIN_19		456	CH_19		
CH_PIN_20		127	CH_20		
CH_PIN_21		94	CH_21		
CH_PIN_24		1005	CH_24		
CH_PIN_25		929	CH_25		

☞ **Components and Electric Circuit → Terminal → New** 

Result (2)

At the creation of these terminals, the algorithm for the creation of connections is automatically run and twenty new equipotential connections between pins and channels have been created by Flux PEEC.

Nevertheless, due to the section dimensions of the pins, it is more advisable to set proximity-type connections in this case, to better represent the real electromagnetic phenomena.

Continued on next page

Data (4)

For a more realistic modeling of the phenomena, connections between channels and pins are modified from equipotential-type to proximity-type. Their properties are presented in the table below.

Connections	
Name	**Terminals connection**
CO_AUTO_36 to CO_AUTO_55	**proximity connection**

☞ **Components and Electric Circuit → Connection → Edit array** 

3.2. Manual creation of connections

Goal

Most of the conductors describing the power module have been automatically connected together by Flux PEEC, as illustrated in the previous chapter.

Nevertheless, some connections have to be established manually by the user, because no intersections exist between the faces of the conductors: it is for example the case of pins and PCB busbars or of some bondings. Sixteen new connections are then created.

Data (1)

The properties of five manually created equipotential connections between pins and PCB busbars are presented in the table below.

Equipotential connections	
Name	**Connected terminals**
PCB_M_TO_PIN21	PCB_M_P21 TERM_PIN_21_1
PCB_M_TO_PIN14	PCB_M_P14 TERM_PIN_14_1
PCB_P_TO_PIN24	PCB_P_P24 TERM_PIN_24_1
PCB_P_TO_PIN25	PCB_P_P25 TERM_PIN_25_1
PCB_P_TO_PIN12	PCB_P_P12 TERM_PIN_12_1

☞ **Components and Electric Circuit → Connection → New** 

Continued on next page

Data (2)

The properties of eleven manually created equipotential connections between bondings are presented in the table below. These connections link internal bondings of the power module in the zones where diode's anodes and IGBT's emitters are located.

Note: no connection is established near the anode of the second low-side diode, because there is no external pin for this signal.

Equipotential connections	
Name	**Connected terminals**
A1H	TERM_BOND_1_4 TERM_BOND_21_1
E1H	TERM_BOND_3_4 TERM_BOND_22_1
A2H	TERM_BOND_4_4 TERM_BOND_23_1
E2H	TERM_BOND_6_4 TERM_BOND_24_1
A3H	TERM_BOND_7_4 TERM_BOND_25_1
E3H	TERM_BOND_9_4 TERM_BOND_26_1
A3L	TERM_BOND_11_4 TERM_BOND_27_1
E3L	TERM_BOND_12_4 TERM_BOND_28_1
E2L	TERM_BOND_14_4 TERM_BOND_30_1
E1L	TERM_BOND_16_4 TERM_BOND_31_1
A1L	TERM_BOND_18_4 TERM_BOND_32_1

☞ **Components and Electric Circuit → Connection → New** 

Action

In order to check if all connections between conductors have been established, it is advisable to run an automatic algorithm able to find out the groups of connected conductors.

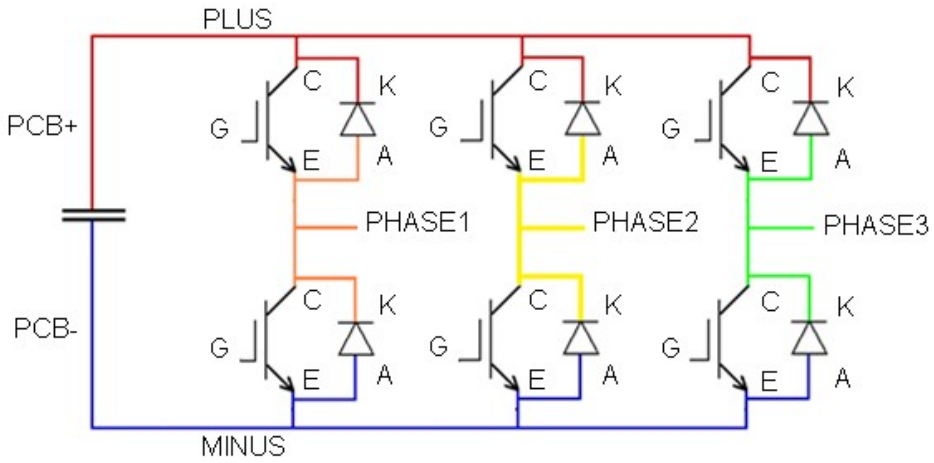
☞ **Components and Electric Circuit → Check groups of connected conductors** 

Continued on next page

Result

In the case studied in this tutorial, twelve groups of connected conductors exist and are detected by the algorithm:

- six correspond to pin, channel and bondings of the gate of the six IGBT; these groups are not linked to the rest of the structure, because the aim of the study is the computation of the loop inductances when a couple of complementary diode/IGBT is short-circuited; nevertheless, eddy currents flow in these conductors and could have an effect on the loop inductances
- one is the heat spreader, which is not connected with any other conductors, but where eddy currents flow
- the other five groups are the main sets of conductors of the power module (PCB_P & PLUS, PCB_M & MINUS, PHASE1, PHASE2 and PHASE3), as represented by different colours in its electrical scheme shown in the figure below



3.3. Definition of the impedance probe

Introduction

Impedance probes are used to compute the values of the equivalent impedance between chosen points of the geometry, as well as to extract macromodels of the simulated structure for system-level computations.

In this tutorial one probe is used to compute the impedance seen from the capacitor bank in order to deduce the switching loop inductances of the power module.

Data

An impedance probe is created and its graphical symbol is positioned in the scheme.

Impedance probe			
Name	Model		
	Graphic description	Positive terminal	Negative terminal
LOOP_PROBE	Location with terminals	PCB_P_IN	PCB_M_IN

☞ Components and Electric Circuit → Impedance probe → New 

Result

Two new equipotential connections have been automatically created by Flux PEEC in order to link the impedance probe to the conductors describing the power module. Their properties are summarized in the table below.

Equipotential connections	
Name	Connected terminals
CO_AUTO_56	TERM_LOOP_PROBE_1 PCB_P_IN
CO_AUTO_57	TERM_LOOP_PROBE_2 PCB_M_IN

4. Computation of loop inductances

Introduction

This chapter explains how to conclude within Flux PEEC the definition of the electric circuit in order to compute the six loop inductances of the power module and how to post-process the results to get the looked-for values.

Overview

The computation of each loop inductance will be realized in three steps listed in the table below.

Stage	Description
1	Definition of the electrical loop
2	Solving process
3	Post-processing

Contents

This chapter contains the following topics:

4.1. Electrical loops

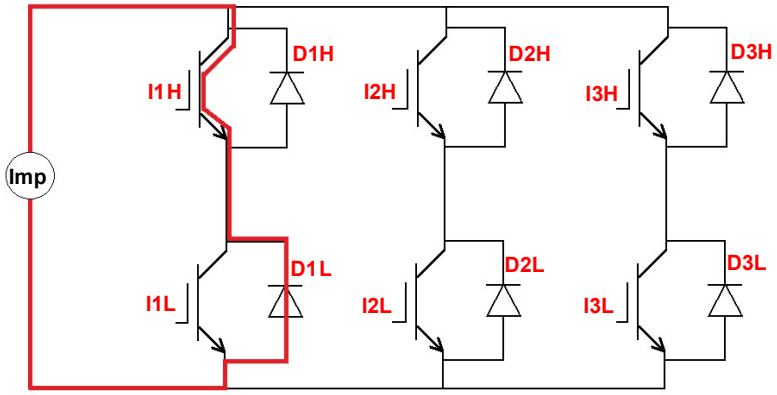
Goal

In order to compute the equivalent inductance of a loop, the electric circuit has to be completed by adequate conductor connections representing the ON-state of diodes and IGBT: a short circuit has to be set up between anode and cathode or between collector and emitter, respectively.

Loop definition

For this power module and its command strategy, one couple of complementary diode/IGBT has to be short-circuited, whereas the five others remain open.

The example of the couple composed by the first high-side IGBT (I1H) and the first low-side diode (D1L) is reported in the figure below. The five other configurations are similar to this one.



Data

For each of the six different configurations, a short circuit has to be set up between anode and cathode of the involved diode and between collector and emitter of the involved IGBT.

Within Flux PEEC two equipotential connections must be modified by adding a terminal; in particular, the connection representing the short circuit at the diode level has to be completed with the terminal corresponding to the cathode, whereas the connection at the IGBT level completed with the collector terminal.

An exception to this action exists because, as explained at page 44, the anode of the second low-side diode is not provided with its external pin. Therefore, the equipotential connection (named A2L) between its anode and its cathode must be created at this stage of the study.

The properties of the connections to be modified (or created: A2L) for each solving case (designated by its Flux PEEC project name) are presented in the table below.

Continued on next page

Equipotential connections			
Couple IGBT/diode	**Flux PEEC project**	**Name**	**Connected terminals**
I1H/D1L	**PowerModule_Switch_1.FLU**	E1H	TERM_BOND_3_4 TERM_BOND_22_1 C1H
		A1L	TERM_BOND_18_4 TERM_BOND_32_1 K1L
I1L/D1H	**PowerModule_Switch_2.FLU**	E1L	TERM_BOND_16_4 TERM_BOND_31_1 C1L
		A1H	TERM_BOND_1_4 TERM_BOND_21_1 K1H
I2H/D2L	**PowerModule_Switch_3.FLU**	E2H	TERM_BOND_6_4 TERM_BOND_24_1 C2H
		A2L	TERM_BOND_29_1 K2L
I2L/D2H	**PowerModule_Switch_4.FLU**	E2L	TERM_BOND_14_4 TERM_BOND_30_1 C2L
		A2H	TERM_BOND_4_4 TERM_BOND_23_1 K2H
I3H/D3L	**PowerModule_Switch_5.FLU**	E3H	TERM_BOND_9_4 TERM_BOND_26_1 C3H
		A3L	TERM_BOND_11_4 TERM_BOND_27_1 K3L
I3L/D3H	**PowerModule_Switch_6.FLU**	E3L	TERM_BOND_12_4 TERM_BOND_28_1 C3L
		A3H	TERM_BOND_7_4 TERM_BOND_25_1 K3H

☞ **Components and Electric Circuit → Connection → Edit** 

4.2. Solving process

Goal

The Flux PEEC project **PowerModule_Switch_X.FLU** (X indicating the computation case) is solved to get the loop inductance.

Action

The command **Solve** launches the impedance computation algorithm according to the solving scenario.

☞	**Solving → Solve**	

Consequence (1)

The solving process consists of two main parts: in the first one, the size of the computed impedance matrix is equal to the number of mesh subdivisions.

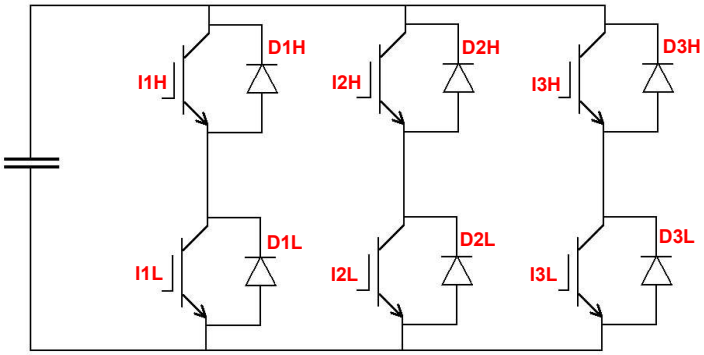
Consequence (2)

In the second part, the size of impedance matrix is reduced to the number of impedance probes, in order to present useful results to the user.

4.3. Obtained results

Goal

The six switching loop inductance values are obtained by means of the impedance probe.



Action (1)

The **Results** tab of the impedance probe contains real and imaginary parts of the equivalent impedance computed by Flux PEEC, as shown in the table below for the loop I1H/D1L (Flux PEEC project: **PowerModule_Switch_1.FLU**).

Impedance probe		
Name	**Re (Impedance) (Ohm)**	**Im (Impedance) (Ohm)**
LOOP_PROBE	0.034160	0.304562

☞ Components and Electric Circuit → Impedance probe → Edit 

Action (2)

To get the switching loop inductance, it is sufficient to divide the imaginary part of the obtained equivalent impedance by the angular frequency ($\omega = 2\pi f$), where f in this study has been set to 1 MHz).

Results

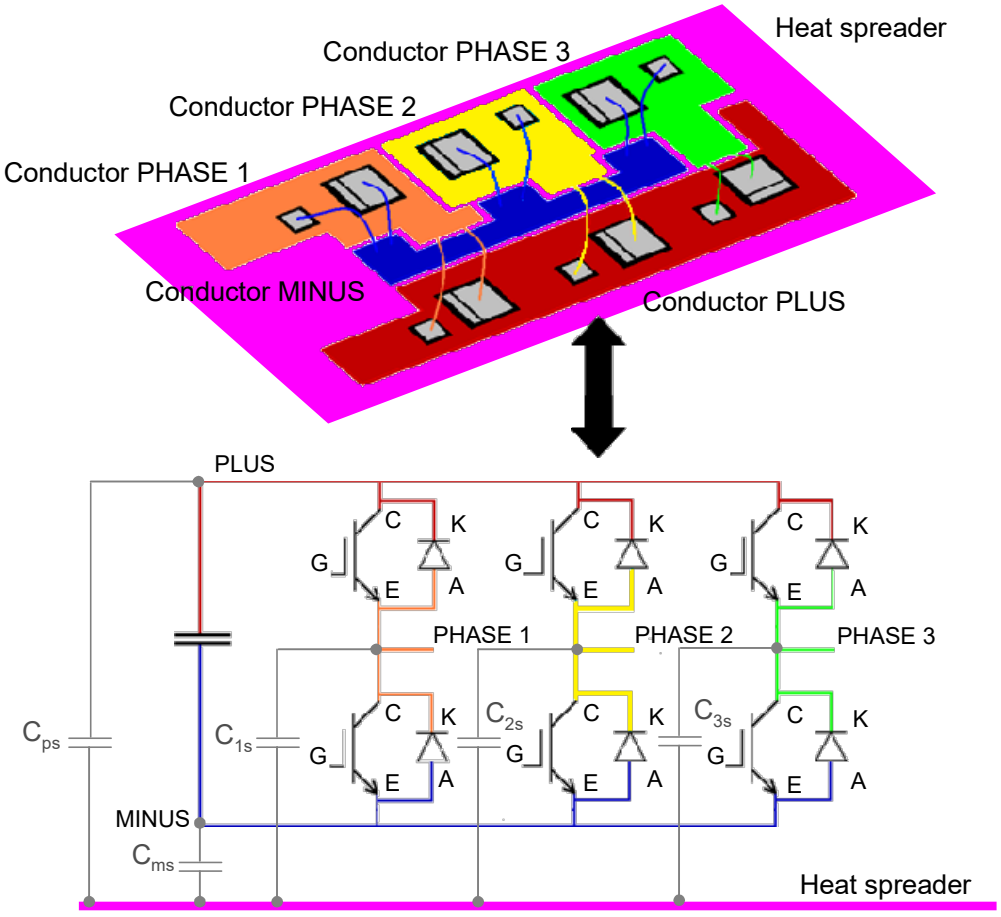
The obtained results for all the six loops (or couples of complementary diode/IGBT) are reported in the table below.

Switching loop results			
Couple IGBT/diode	**Equivalent impedance**		**Loop inductance (nH)**
	Real part (Ω)	**Imaginary part (Ω)**	
I1H-D1L	0.034160	0.304562	48.47
I1L-D1H	0.039019	0.326884	52.03
I2H-D2L	0.041313	0.326692	51.99
I2L-D2H	0.037950	0.333307	53.05
I3H-D3L	0.027413	0.264361	42.07
I3L-D3H	0.036412	0.304191	48.41

Continued on next page

Conclusion

Loop inductances of the power module have been computed by means of this Flux PEEC model, which can be considered as the starting point for enhanced EMC analysis. For example, as shown in the figure below, stray capacitances can be included in the simulation to study common-mode currents: to perform such characterizations the Flux PEEC model should be completed with further terminals associated to the heat spreader and so on.



5. Inclusion of parasitic capacitances in the model

Introduction

This chapter explains how to include the computation of parasitic capacitances into the previously-established Flux PEEC models.

The evaluation of the input impedance of the power module with respect to frequency is also presented for all the six configurations already considered in chapter 4.

Overview

The inclusion of the parasitic capacitances for the computation of the input impedances will be realized in seven steps listed in the table below.

Stage	Description
1	Application and scenario changing
2	Definition of dielectrics
3	Definition of capacitive regions
4	Computation of capacitance matrices
5	Definition of the electrical loop
6	Connection of capacitors and solving process
7	Post-processing

Contents

This chapter contains the following topics:

5.1. Application and scenario changing

Goal (1)

Computation of parasitic capacitances of the structure need to use the Flux PEEC application called "**Conductor impedances with capacitive effects**".

On the other hand, geometry, physics and electrical properties of conductors and components can be maintained; consequently this chapter starts from the Flux PEEC project obtained at the end of chapter 3. The reader willing to recover this project has just to run the Python file ***State_Circuit.py*** provided in the folder

…\flux\Flux\DocExamples\ExamplesPEEC\Tutorial_Technical\PowerModule\PowerModule.zip\PowerModule_PEEC_Case1

Python file

The reader willing to skip this part of the tutorial and to directly move to the solving process (paragraph 5.5) has just to run the Python file ***buildCircuit2.py*** provided in the folder

…\flux\Flux\DocExamples\ExamplesPEEC\Tutorial_Technical\PowerModule\PowerModule.zip\PowerModule_PEEC_Case2

Definition of the application

The suitable application is **Conductor impedances with capacitive effects**. Properties to be set are presented in the table below.

Type of application	Default material for new conductors
Conductor impedances with capacitive effects	copper

☞ Application → Edit current application

Goal (2)

For the evaluation of the input impedances over a large frequency range, from low (some kHz) to high (some hundreds of MHz) frequencies, the solving scenario need to be adapted from a "Mono-value" type to "**Multi-values**".

Definition of the scenario

Properties of the new scenario are reported in the table below.

Solving scenario					
Controlled parameter	Control type	Parameter control			
		Lower limit	Higher limit	Variation method	Step number
FREQUENCY	Multi-values	1e3	10e6	Step number (**log**)	21
		10e6	80e6	Step number (**lin**)	8
		80e6	120e6	Step number (**lin**)	21
		120e6	200e6	Step number (**lin**)	11

☞ Solving → Solving scenario → Edit 

5.2. Definition of dielectrics

Introduction

Values of parasitic capacitances depend on geometry and position of conductors, but also on the presence of dielectric materials in the neighborhoods.

In the considered power module, two dielectrics exist and are to be modeled: one is the silicon within the conductors of the PCB busbar, and second is the resin layer between the heat spreader and the DBC substrate.

Goal

Define the geometry and the physics for dielectrics, including their materials and meshing properties.

Action

To build the dielectric geometries, the project needs to be unmeshed.

☞ **Solving → Delete meshing** 

Geometrical data (1)

The geometrical definition of a dielectric is based on volumes.

The volume for the dielectric inside the busbar does not exist in the Flux PEEC project: it needs to be created by means of points, lines and faces.

The properties of the eight new points necessary for the definition of this first dielectric are reported in the table below.

Point defined by its **parametric coordinates**				
Number	**Geometric definition**			
	Coordinate system	**Coordinates**		
		First	**Second**	**Third**
1234	XYZ1	13.21	-41.605	9.15
1235		-19.8	-41.605	9.15
1236		-19.8	34.545	9.15
1237		13.21	34.545	9.15
1238		13.21	-41.605	9.85
1239		-19.8	-41.605	9.85
1240		-19.8	34.545	9.85
1241		13.21	34.545	9.85

☞ **Geometry → Assimilation geometry → Point → New** 

Continued on next page

Geometrical data (2)

Created points have to be joined by segment-type lines.

The properties of the sixteen new lines necessary for the definition of the first dielectric are reported in the table below.

Segment defined by **Starting** and **Ending Points**		
Number	**Points defining segment**	
1947	2	1234
1948	1234	1237
1949	1237	1236
1950	1236	4
1951	5	1235
1952	1235	1
1953	1234	1238
1954	1237	1241
1955	1236	1240
1956	1235	1239
1957	1239	1238
1958	1238	736
1959	735	1241
1960	1241	734
1961	740	1240
1962	1240	1239

☞ **Geometry → Assimilation geometry → Line → New** 

Geometrical action (1)

Creation of faces is now possible using the algorithm of automatic construction.

Eight new faces are automatically built by Flux PEEC.

☞ **Geometry → Assimilation geometry → Face → Build faces** 

Geometrical action (2)

Creation of volumes is now possible using the algorithm of automatic construction.

One new volume is automatically built by Flux PEEC.

☞ **Geometry → Assimilation geometry → Volume → Build volumes** 

Continued on next page

Physics of busbar silicon

The created volume enables the definition of the first dielectric of the studied system: the busbar silicon. Its material is epoxy, which is predefined in the Flux PEEC environment and whose relative permittivity is equal to 4.3

The properties of this first dielectric are reported in the table below.

Dielectric defined by a **list of volumes**						
Name	**Description**	**Meshing**				**Material**
	Volumes	**Type**	**Shape**	**Definition**	**Size value (mm)**	
SILICON	181	Uniform regular	Quadrangle	Absolute	2	EPOXY

☞ **Physics → Dielectric → New** 

Physical action

For the second dielectric (the resin layer between the heat spreader and the DBC substrate), volumes already exist since they have been imported by CAD file at the beginning of this tutorial. On the other hand, material is a particular resin, whose relative permittivity is equal to 9.5, which needs to be manually created by the user.

The properties of this material are reported in the table below.

Dielectric material		
Name	**D(E)**	
	Dielectric property	**Relative permittivity**
RESIN	Linear isotropic	9.5

☞ **Physics→ Material → New** 

Physics of resin layer

Definition of the second dielectric of the studied system is now possible.

The properties of this dielectric are reported in the table below.

Dielectric defined by a **list of volumes**						
Name	**Description**	**Meshing**				**Material**
	Volumes	**Type**	**Shape**	**Definition**	**Size value (mm)**	
LAYER	178	Uniform regular	Quadrangle	Absolute	2	RESIN

☞ **Physics → Dielectric → New** 

5.3. Definition of capacitive regions

Introduction

Computation of parasitic capacitances between conductors, in the Flux PEEC environment, is based on the concept of capacitive regions. A capacitive region is an area where voltage can be considered uniform, i.e. $\Delta V \approx 0$

Inside Flux PEEC, a **capacitive region** is defined by one or several conductors, either unidirectional or bidirectional. Since it is not mandatory that all conductors belong to a capacitive region, the user can eventually decide by himself the list of conductors between which compute parasitic capacitances and so save computation time by discarding useless parts.

In fact, capacitances are more important between conductors which have a large surface facing each other, while the effect of smallest conductors can often be neglected. For example in this study, eight conductors appear as dominant: the two conductors of the PCB busbar, the five conductors (phase1, phase2, phase3, plus, minus) of the DBC substrate and the heat spreader.

Goal

Define the physics for capacitive regions, including their meshing properties.

Physical data

The properties of capacitive regions to be defined are reported in the table below.

Capacitive regions defined by a **list of conductors**						
Name	**Description**		**Meshing**			
	Unidirectional conductors	**Bidirectional conductors**	**Type**	**Shape**	**Definition**	**Size value (mm)**
PCB_P	/	PCB_P	Uniform regular	Quadrangle	Absolute	2
PCB_M	/	PCB_M	Uniform regular	Quadrangle	Absolute	2
PHASE1	/	PHASE1	Uniform regular	Quadrangle	Absolute	2
PHASE2	/	PHASE2	Uniform regular	Quadrangle	Absolute	2
PHASE3	/	PHASE3	Uniform regular	Quadrangle	Absolute	2
PLUS	/	PLUS	Uniform regular	Quadrangle	Absolute	2
MINUS	/	MINUS	Uniform regular	Quadrangle	Absolute	2
HEAT	/	HEAT	Uniform regular	Quadrangle	Absolute	2

☞ **Physics → Capacitive region→ New** 

Continued on next page

Note

Once parasitic capacitance matrix will be computed, it will be necessary to transform these values into equivalent capacitors and connect them to existing conductors in order to evaluate the input impedance of the power module.

Connection of components with conductors need that all involved conductors have at least a terminal; this is not yet the case for the heat spreader. Two point-type terminals are now created to enable the future connection (paragraph 5.5) of the parasitic capacitances to the heat spreader.

Data (1)

The properties of the points necessary for the definition of the terminals of HEAT conductor are reported in the table below.

Point defined by its **parametric coordinates**					
Number	**Geometric definition**				**Appearance**
	Coord. system	**Coordinates**			**Color**
		First	**Second**	**Third**	
1242	XYZ1	0	-15	-8	Magenta
1243		0	25	-8	

☞ **Geometry → Assimilation geometry → Point → New** 

Data (2)

The properties of terminals of HEAT conductor are reported in the table below.

Terminal of **bidirectional conductor**					
Name	**Definition**				**Appearance**
	Type of terminal	**Point or faces of the terminal**	**Conductor where the terminal is located**	**Pin of macro component**	**Color**
HEAT_1	Point	1242	HEAT	No	Magenta
HEAT_2		1243			

☞ **Components and Electric Circuit → Terminal → New** 

5.4. Computation of capacitance matrices

Introduction

Since a parasitic capacitance exists between each pair of conductors (capacitive regions inside Flux PEEC), it is suitable to organize them in a square matrix, which will be symmetric and constituted by real numbers.

Three different capacitance matrices can be identified:

- **Maxwell matrix**, which contains the results of a classical electrostatic simulation and expresses the relationship between the voltage of all conductors V and their electrical charge Q;
- **Kirchhoff matrix**, obtained from the Maxwell one, contains the mutual capacitances between conductors and their self capacitance with respect to a voltage reference point placed at infinite;
- **Capacitance matrix**, obtained from the Kirchhoff one, is the most practical representation, since the effect of self-capacitances is included into mutual values which definitely express the real capacitances between conductors (capacitive regions inside Flux PEEC).

In Flux PEEC computation of these matrices requires to mesh dielectrics and capacitive regions.

Action: mesh

The meshing for capacitive computation is different from the inductive one shown in paragraph 2.3.4 of this tutorial.

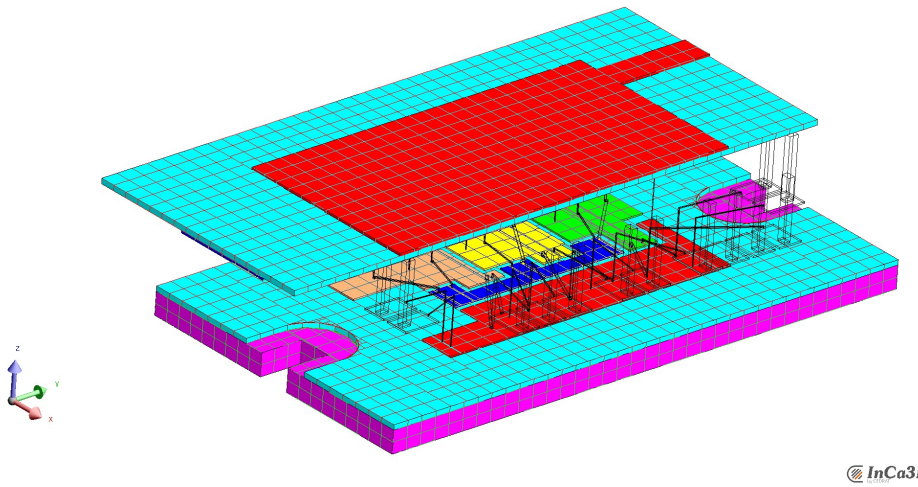
It is generated using the command **Mesh dielectrics and capacitive regions**.

☞	Parasitic Capacitances → Mesh dielectrics and capacitive regions	

Result: meshing

Obtained meshing is shown in the figure below.

Note: only dielectrics (in turquoise) and capacitive regions are meshed, while other conductors not belonging to any capacitive region are unmeshed, because they will not be involved in this computation.



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Action: compute C matrices

The command **Compute capacitance matrix** launches the algorithms for the evaluation of the three capacitance matrices.

☞ Parasitic Capacitances → Compute capacitance matrix	

Result: C matrices

The three matrices (Maxwell, Kirchhoff and Capacitance) are stored in the data tree, in the folder *Components*. Their values can be displayed or written in an external TXT file.

☞ Parasitic Capacitances → Parasitic capacitance matrix → Write matrix in file	

For example, obtained **Capacitance matrix** values expressed in pF are reported in the table below. Note that the matrix is symmetric and diagonal elements are equal to zero.

Parasitic **capacitance matrix** between regions, values in **pF**								
	PCB_P	**PCB_M**	**PHASE1**	**PHASE2**	**PHASE3**	**PLUS**	**MINUS**	**HEAT**
PCB_P	0	56.46	4.15e-3	4.03e-3	8.93e-3	65.09e-3	7.99e-3	755.6e-3
PCB_M	56.46	0	83.07e-3	68.96e-3	63.49e-3	120.3e-3	49.27e-3	1.462
PHASE1	4.15e-3	83.07e-3	0	64.74e-3	0.834e-3	11.07e-3	54.00e-3	18.66
PHASE2	4.03e-3	68.96e-3	64.74e-3	0	75.32e-3	13.73e-3	60.79e-3	15.81
PHASE3	8.93e-3	63.49e-3	0.834e-3	75.32e-3	0	7.35e-3	23.08e-3	16.42
PLUS	65.09e-3	120.3e-3	11.07e-3	13.73e-3	7.35e-3	0	37.77e-3	44.33
MINUS	7.99e-3	49.27e-3	54.00e-3	60.79e-3	23.08e-3	37.77e-3	0	12.33
HEAT	755.6e-3	1.462	18.66	15.81	16.42	44.33	12.33	0

5.5. Electrical loops for input impedances

Introduction

Values of parasitic capacitances do not depend on the external circuit (sources and loads) connected to conductors of the studied system, but it is strongly advised to **transform capacitance matrix into capacitors connected to conductors only after having completed the description of the circuit**. In fact, connection locations of parasitic capacitors can be influenced by existing connections between conductors and external components.

Consequently, in this paragraph the definition of the electrical loops for the computation of the input impedance of the power module is carried out before the inclusion of parasitic capacitances in the model.

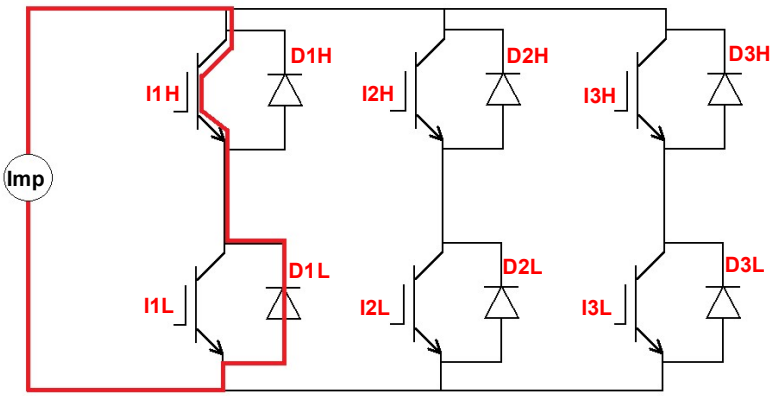
Goal

In the same manner as the evaluation of loop inductances performed in chapter 4, the computation of the input impedance with respect to the frequency needs to complete the electric circuit by adequate conductor connections representing the ON-state of diodes and IGBT: a short circuit has to be set up between anode and cathode or between collector and emitter, respectively.

Definition of the input impedances

The input impedance of this power module will be computed in the same six electrical configurations considered in chapter 4: one couple of complementary diode/IGBT will be short-circuited, whereas the five others will remain open.

The example of the couple composed by the first high-side IGBT (I1H) and the first low-side diode (D1L) is reported in the figure below. The five other configurations are similar to this one.



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Data

To prepare each of the six different configurations, in the same way as in chapter 4 for the computation of loop inductances, two equipotential connections must be modified within Flux PEEC by adding a terminal.

The connection representing the short circuit at the diode level has to be completed with the terminal corresponding to the cathode, whereas the connection at the IGBT level with the collector terminal. The exception is always the third configuration since the connection named A2L between the anode and the cathode of the second low-side diode must be created at this stage of the study.

The properties of the connections to be modified (or created: A2L) for each solving case (designated by its Flux PEEC project name) are presented in the table below.

Equipotential connections			
Couple IGBT/diode	**Flux PEEC project**	**Name**	**Connected terminals**
I1H/D1L	**PowerModule_Switch_C_1.FLU**	E1H	TERM_BOND_3_4 TERM_BOND_22_1 C1H
		A1L	TERM_BOND_18_4 TERM_BOND_32_1 K1L
I1L/D1H	**PowerModule_Switch_C_2.FLU**	E1L	TERM_BOND_16_4 TERM_BOND_31_1 C1L
		A1H	TERM_BOND_1_4 TERM_BOND_21_1 K1H
I2H/D2L	**PowerModule_Switch_C_3.FLU**	E2H	TERM_BOND_6_4 TERM_BOND_24_1 C2H
		A2L	TERM_BOND_29_1 K2L
I2L/D2H	**PowerModule_Switch_C_4.FLU**	E2L	TERM_BOND_14_4 TERM_BOND_30_1 C2L
		A2H	TERM_BOND_4_4 TERM_BOND_23_1 K2H
I3H/D3L	**PowerModule_Switch_C_5.FLU**	E3H	TERM_BOND_9_4 TERM_BOND_26_1 C3H
		A3L	TERM_BOND_11_4 TERM_BOND_27_1 K3L
I3L/D3H	**PowerModule_Switch_C_6.FLU**	E3L	TERM_BOND_12_4 TERM_BOND_28_1 C3L
		A3H	TERM_BOND_7_4 TERM_BOND_25_1 K3H

☞ **Components and Electric Circuit → Connection → Edit** 

5.6. Connection of capacitors and solving process

Goal

The Flux PEEC project **PowerModule_Switch_C_X.FLU** (X indicating the computation case) is completed with the inclusion of parasitic capacitors, and then solved to get the input impedance of the power module.

Action (1)

Creation of equivalent capacitors representing the values of the parasitic capacitance matrices and their connection to existing conductors has to be carried out by the command **Create and connect capacitors to conductors** which automatically launches the corresponding algorithm.

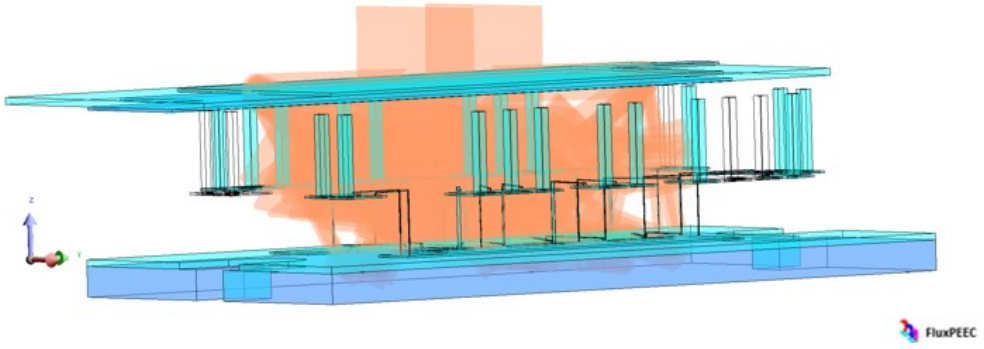
The properties to be used in this study are presented in the table below.

Create and connect capacitors to conductors	
Parasitic capacitance matrix	CAPACITANCE
Connection type for capacitors	PI
Threshold value	1.0e-18
Addition type	by connection
Force the use of…	yes
Visualize created capacitors	yes

☞ **Parasitic Capacitances → Create and connect capacitors to conductors** 

Result

Fifty-five capacitors are created: they appear in the data tree in the folder *Components/RLC components*
They are connected between corresponding conductors and are visible (in orange), as shown in the figure below.



Action (2)

The project is ready to be solved.
The command **Solve** launches the impedance computation algorithm according to the solving scenario.

☞ **Solving → Solve** 

5.7. Obtained results

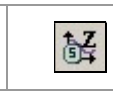
Goal

The input impedance for the six switching configuration are obtained by means of the impedance probe.

Action

The **Magnitude** (the phase as well as the real and imaginary parts) of the input impedance computed by Flux PEEC is displayed as function of the frequency by means of a 2D curve.

☞ **Post Processing → Curves → 2D curve (parameter) → Impedance between probes**



Result

The obtained curve for the first configuration (Flux PEEC project: **PowerModule_Switch_C_1.FLU**) is reported in the figure below.

It has to be noted that resonance at the frequency of 95 MHz is caused by the inclusion of the capacitive effects into the resistive-inductive model.